REMARKS

Claims 1-30 are pending in the present application and were examined. Claims 1-2, 14, 19, 21-23 and 25-30 stand rejected and Claims 13, 15-18, 20 and 24 are objected to. In response, Claims 1, 4-6, 11, 21 and 24-26 are amended, Claim 22 is cancelled and Claim 31 is added. Applicants respectfully request reconsideration of pending Claims 1-21 and 23-31 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Objection to the Abstract

The Examiner has objected to the Abstract for a typographical error. Applicants have amended the Abstract in accordance with the Examiner's objection and attach a replacement Abstract to this Response. Therefore, Applicants request that the Examiner withdraw the objection to the Abstract.

II. Objection to the Specification

The Examiner has objected to the specification for various informalities. Applicants have amended the specification in accordance with the Examiner's objection. Therefore, Applicants request that the Examiner withdraw the objection to the Specification.

III. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1, 4, 6, 9, 11, 21 and 22 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application No. 2004/0205298 of Bearden et al. ("Bearden"). Applicants respectfully traverse this rejection.

Regarding Claims 1 and 6, Claims 1 and 6 are amended to recite the following claim features, which are neither disclosed nor suggested by Bearden:

> identifying a prefetch depth;
> detecting a memory subsystem response level according to at least one bus transaction directed to a main memory;
> prefetching data according to an adjusted prefetch depth; and
> adjusting the prefetch depth as changes in the memory subsystem response level are detected. (Emphasis added.)

As indicated by the above-recited features of amended Claims 1 and 6, a prefetch depth is adjusted based on a detected memory subsystem response level according to at least

one bus transaction directed to a main memory. Applicants respectfully submit that the main memory, as recited by amended Claims 1 and 6, refers to main memory of a computer system, which is known to those skilled in the art and as indicated by the attached *WEBOPEDIA* definition (Exhibit "A"), generally refers to physical memory that is internal to a computer, such that the word "main" is used to distinguish it from external mass storage devices, such as disk drives, for example, as described within Bearden.

In contrast to the above-recited features of amended Claims 1 and 6, the disclosure in Bearden is directed to:

> Computer data storage devices, such as disk drives and Redundant Array of Independent Disks (RAID), typically use a cache memory in combination with mass storage media (e.g., magnetic tape or disk) to save and retrieve data in response to requests from a host device. (pg. 1, ¶003, lines 1-5.) (Emphasis added.)

In other words, detecting of the memory subsystem response level according to at least one bus transaction directed to a main memory, as recited by amended Claims 1 and 6, determine a memory subsystem response level according to the internal memory of a computer system. Conversely, the disclosure in Bearden is directed to mass storage devices, which are used for external memory. As disclosed by Bearden:

> The system environment 100 of FIG. 1 includes a storage device 102 operatively coupled to one or more host device(s) 104 through a communications channel 106. The communications channel 106 can be wired or wireless and can include, for example, a LAN (local area network), a WAN (wide area network), an intranet, the Internet, an extranet, a fiber optic cable link, a direct connection, or any other suitable communication link. (pg. 2, ¶0024, lines 1-8.) (Emphasis added.)

The above-described features recited by amended Claims 1 and 6 are taken from Claim 11. As indicated by the Examiner regarding the rejection of Claim 11, as well as Claims 14 and 19:

> Bearden teaches the operational parameter generator looks up a disk drive latency, cache capacity to adjust the prefetch depth (paragraph [0061], lines 4-8 and paragraph [0067], lines 7-10) and hence teaches the tracking of memory subsystem response level (paragraph [0062]) and requests and occupancy level. (pg. 3, ¶3 of the Office Action mailed October 14, 2005.) (Emphasis added.)

Applicants respectfully submit that the disk drive latency and cache capacity, as referred to by the Examiner, do not refer to the tracking of a memory subsystem response

level and requests and an occupancy level, as indicated by the Examiner. In contrast, as explicitly disclosed by Bearden:

> Generally, accessing the disk(s) 240 is a relatively time-consuming task in the disk drive 202. The time-consuming nature of accessing (i.e., reading and writing) the disk(s) 240 is at least partly due to the electromechanical processes of positioning the disk(s) 240 and positioning the actuator arm. Time latencies that are characteristic of accessing the disk(2) 240 are more or less exhibited by other types of mass storage devices that access mass storage media, such as tape drives, optical storage devices, and the like.
>
> As a result, mass storage devices, such as the disk drive 202, may employ cache memory to facilitate rapid data I/O responses to the host 204. (pg. 3, ¶¶0037-0038.) (Emphasis added.)

In other words, as indicated by the attached *WEBOPEDIA* definition of "latency" (Exhibit "B"), the latency or disk drive latency referred to by Bearden is generally defined as the time it takes to position the proper sector under the read/write head, as required to access data.

As further indicated by Bearden, such operational parameters, such as disk drive latency, may change, for example, if one disk drive model or type is substituted for another, or as indicated, a response rate may decrease if errors of the disk media result in increased retries to obtain valid data. (*See*, ¶0062, pg. 6, lines 1-8 of Bearden.) Hence, Applicants respectfully submit that the operational parameters referred to by the Examiner are strictly limited to characteristics of the mass storage devices or disk drives, as disclosed in Bearden, and are not based on pending transaction requests directed to main memory for detection of a memory subsystem response level, as recited by amended Claims 1 and 6.

As mandated by case law, "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), 730 F.2d 452, 1458 (Fed. Cir. 1994) (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, amended Claims 1 and 6 recite detection of a memory subsystem response level according to at least one bus transaction directed to a main memory. Conversely, Bearden is directed to adjusting a prefetch depth for prefetching data within a cache memory that is located on an external mass storage device. (pg. 3, ¶0038.)

As disclosed by Bearden, the operational parameters which are used to adjust the prefetch depth are based solely on characteristics of the disk drive. Hence, Bearden fails to disclose or suggest the detection of a memory subsystem response level according to at least one bus transaction directed to a main memory, as recited by amended Claims 1 and 6.

Furthermore as indicated, based on the definition provided above by *WEBOPEDIA* regarding main memory, main memory generally refers to the internal memory of a computer system. (*See*, Exhibit A.) Consequently, the disclosure in Bearden is directed to external, or mass storage devices, such as disk memory. (pg. 3, ¶¶0037-0038.) Conversely, as recited by amended Claims 1 and 6, a memory subsystem response level is detected according to at least one bus transaction directed to a main memory.

Therefore, Applicants respectfully submit that the Examiner is prohibited from relying on Bearden as an anticipatory reference since Bearden fails to exactly disclose each and every element as recited by amended Claims 1 and 6; specifically, the detection of a memory subsystem response level, according to at least one bus transaction, directed to a main memory. Banner Titanium, supra. Consequently, Applicants respectfully submit that the Examiner fails to illustrate that the single prior art reference disclosure of Bearden includes the presence of each and every element of amended Claims 1 and 6, as arranged in amended Claims 1 and 6, respectively, and required to establish a *prima facie* case of anticipation. Lindemann, supra.

Accordingly, Applicants respectfully submit that Claims 1 and 6, as amended, are patentable over Bearden, as well as the references of record. Id. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 1 and 6, as amended.

Regarding Claim 4, Claim 4, based on its dependency from Claim 1, is also patentable over Bearden, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 4.

Regarding Claim 9, Claim 9, based on its dependency from Claim 6, is also patentable over Bearden, as well as the references of record. Consequently, Applicants

respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 9.

Regarding Claim 11, Claim 11 recites analogous claim features to amended Claims 1 and 6. Consequently, Applicants' arguments provided above with regard to the §102(e) rejection of Claims 1 and 6 equally apply to the Examiner's §102(e) rejection of Claim 11 as anticipated by Bearden.

Accordingly, for at least the reasons provided above, Applicants respectfully submit that the Examiner is prohibited from relying on Bearden as an anticipatory reference, since Bearden fails to exactly disclose each and every element recited by amended Claim 11, and specifically, the detection of a memory subsystem responsible according to at least one bus transaction directed to a main memory. Consequently, Applicants respectfully submit that the Examiner fails to illustrate that the single prior art reference disclosure of Bearden includes the presence of each and element of amended Claim 11, as arranged in Claim 11, and required to establish a *prima facie* case of anticipation. Lindemann, supra.

Accordingly, for at least the reasons provided above, Claim 11, as amended, is patentable over Bearden, as well as the references of record. Id. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 11.

Regarding Claims 14 and 19, Claims 14 and 19, based on their dependency from Claim 11, are also patentable over Bearden, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 14 and 19.

Regarding Claim 21, Claim 21 is amended to recite:

> prefetch control logic to identify a prefetch depth, to prefetch data from a main memory to store the prefetch data within a cache memory according to the identified prefetch depth, and to adjust the prefetch of data as changes in prefetch depth are detected; and
>
> prefetch depth logic to detect a memory subsystem response level according to at least one bus transaction directed to a main memory, and to adjust a prefetch depth according to the detected memory subsystem response level. (Emphasis added.)

Claim 21, as amended, also includes prefetch depth logic, which detects memory subsystem response level according to at least one bus transaction directed to a main

memory, which is analogous to the above-recited features of amended Claim 11. Consequently, for at least the reasons described above with regard to Claims 1, 6 and 11, Applicants respectfully submit that the Examiner is prohibited from relying on Bearden as an anticipatory reference, since Bearden fails to exactly disclose each and every element recited by amended Claim 21. Banner Titanium, supra.

Therefore, Applicants respectfully submit that the Examiner cannot illustrate that the single prior art reference disclosure of Bearden includes the presence of each and every element recited by amended Claim 21, as arranged in amended Claim 21 and required to establish a *prima facie* case of anticipation. Lindemann, supra.

Accordingly, for at least the reasons described above, Claim 21, as amended, is patentable over Bearden, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of amended Claim 21.

Regarding Claim 22, Claim 22, based on its dependency from Claim 21, and for at least the reasons described above, is also patentable over Bearden, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 22.

IV. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 2-3, 5, 7-8, 10, 12 and 23 under 35 U.S.C. §103(a) as being unpatentable over Bearden in view of U.S. Patent Application No. 2004/0148470 of Schulz ("Schulz"). Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of Schulz, Applicants respectfully submit that the Examiner of Schulz fails to rectify the deficiencies of Bearden in teaching or suggesting the detection of a memory subsystem response level according to at least one bus transaction directed to a main memory. Accordingly, for at least the reasons provided above, Applicants respectfully submit that independent Claims 1, 11 and 21 are patentable over the combination of Bearden in view of Schulz, since the combination of Bearden in view of Schultz fails to teach or suggest each and every element recited by independent Claims 1, 6, 11 and 21, as required to establish a *prima facie* case of anticipation. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Accordingly, Claims 2-3 and 5, based on their dependency from Claim 1, are also patentable over the combination of Bearden in view of Schulz. Id. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2-3 and 5.

Regarding Claims 7-8 and 10, Claims 7-8 and 10, based on their dependency from Claim 6, are also patentable over the combination of Bearden in view of Schulz. Id. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 7-8 and 10.

Regarding Claim 23, Claim 23, based on their dependency from Claim 12, for at least the reasons described above, is also patentable over the combination of Bearden in view of Schulz. Id. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 23.

Regarding Claim 26, Claim 26, as amended, recites the following claim feature, which is neither disclosed nor suggested by the combination of Bearden in view of Schulz:

> a processor coupled to the memory controller, the processor including:
> at least one cache memory,
> prefetch control logic to identify a prefetch depth, to prefetch data from the main memory to store the prefetch data within the cache memory according to the identified prefetch depth and to adjust the prefetch of data as changes in prefetch depth are detected, and
> prefetch depth adjustment logic to detect, during prefetch of data, a memory subsystem response level according to at least one bus transaction directed to the main memory, and to adjust a prefetch depth according to the detected memory subsystem response level. (Emphasis added.)

In contrast to the above-recited features of amended Claim 26, as disclosed by Bearden, for example as shown in FIGS. 2-4, a disk drive/array storage device includes a prefetched depth adapter 234/334. Representatively, the host device 204/304, as illustrated in FIGS. 2 and 3 of Bearden, illustrate a CPU 208/308, which neither includes a cache memory nor prefetch depth adapter 234/334. Furthermore, as disclosed by Bearden:

> For ease of description of the system 400, system 400 is described as it may execute within a storage device such as disk drive 202 of FIG. 2 or the RAID device 302 of FIG. 3. (pg. 6, ¶0059, lines 6-9.)

Conversely, amended Claim 26 recites a processor including a cache memory, prefetch control logic and the prefetch depth adjustment logic. Moreover, Applicants

respectfully submit that the above-recited features of amended Claim 26 are analogous to the above-recited features of amended Claims 1, 6, 11 and 21. Consequently, for at least the reasons indicated above, Applicants respectfully submit that the Examiner's citing of Schulz fails to rectify the deficiencies of Bearden to teach such prefetch depth adjustment logic, as recited by Claim 26.

Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of amended Claim 26, since the prior art combination of Bearden in view of Schulz, as well as the references of record, fails to teach each and every element recited by amended Claim 26. In re Royka, supra.

Consequently, Applicants respectfully submit that Claim 26, as amended, is patentable over the combination of Bearden in view of Schulz. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 26.

Regarding Claims 27-30, Claims 27-30, based on their dependency from Claim 26, as amended, and for at least the reasons described above, are also patentable over the combination of Bearden in view of Schulz. Id. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 27-30.

Regarding new Claim 31, new Claim 31 combines the features of Claims 11 and 16, which, as indicated by the Examiner, when combined, result in allowable subject matter. Consequently, Applicants respectfully request that the Examiner allow new Claim 31.

V. Allowable Subject Matter

The Examiner has indicated that Claims 13, 15-18 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicants respectfully thank the Examiner for recognizing the allowability of Claims 13, 15-18 and 24. However, such claims are also allowable based on their dependency from Claims 18 and 21, respectively, for at least the reasons described above.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-21 and 23-31, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: January 17, 2006

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 17, 2006

_____
Marilyn Bass January 17, 2006

Attachments: Replacement Abstract
Ex. A: *WEPODEDIA* definition of "main memory"
Ex. B: *WEBOPEDIA* definition of "latency"

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main memory

Last modified: Tuesday, January 15, 2002

Refers to physical memory that is internal to the computer. The word *main* is used to distinguish it from external mass storage devices such as disk drives. Another term for main memory is *RAM*.

The computer can manipulate only data that is in main memory. Therefore, every program you execute and every file you access must be copied from a storage device into main memory. The amount of main memory on a computer is crucial because it determines how many programs can be executed at one time and how much data can be readily available to a program.

Because computers often have too little main memory to hold all the data they need, computer engineers invented a technique called *swapping*, in which portions of data are copied into main memory as they are needed. Swapping occurs when there is no room in memory for needed data. When one portion of data is copied into memory, an equal-sized portion is copied (swapped) out to make room.

Now, most PCs come with a minimum of 32 megabytes of main memory. You can usually increase the amount of memory by inserting extra memory in the form of chips.

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latency

Last modified: Wednesday, June 23, 2004

(1) In general, the period of time that one component in a system is spinning its wheels waiting for another component. Latency, therefore, is wasted time. For example, in accessing data on a disk, latency is defined as the time it takes to position the proper sector under the read/write head.

(2) In networking, the amount of time it takes a packet to travel from source to destination. Together, latency and bandwidth define the speed and capacity of a network.

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